УДК 621.398.724

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THE OPTOELECTRONIC COMPLEMENTARY DUAL NEURAL ELEMENTS FOR THE IMPLEMENTATION OF NORMALIZED VECTOR "EQUIVALENCE – NONEQUIVALENCE" OPERATIONS

Equivalence models (EM) advantages of neural networks (NN) are shown in paper. EMs are based on vector-matrix procedures with basic operations of continuous neurologic: normalized vector operations "equivalence", "nonequivalence". The capacity of NN on the basis of EM and of its modifications, including auto-and heteroassociative memories for 2D images, exceeds in several times quantity of neurons. Such neuroparadigms are very perspective for processing, recognition, storing large size and strongly correlated images. A biologically motivated concept and time-pulse encoding principles of continuous logic photocurrent mirrors and sample-storage devices with pulse-width photoconverters have allowed us to design generalized structures for realization of the family of normalized linear vector operations "equivalence"-"nonequivalence". Simulation results show, that processing time in such circuits does not exceed units of micro seconds. Circuits are simple, have low supply voltage (1-3)V, low power consumption (milliwatts), low levels of input signals (microwatts), integrated construction, satisfy the problem of interconnections and cascading.

Keywords: *optoelectronic neural networks, time-pulse coded signals, matrix optoelectronic computing, equivalence and nonequivalence operations, photocurrent mirrors, continuous logic.*

Introduction

The decision of basic part of practical tasks by ANN is provided with use of business software, because software creation is more economical and flexible process. However in certain situations the only specialized hardware can suit and offer noticeable advantages. Reasons which compel to search new hardware representations are: speed and productivity due to parallel calculations possibility, system cost declines, more high reliability of functioning, less probability of refuse, safety, special operating descriptions (weight, sizes et cetera). Among plenty of types of devices for ANN design, which divided into three classes, namely: neurocomputers, accelerators for personal computers (PC accelerators) or built-in microcomputers (embedded microcomputers), chips, a substantial role is played by the specialized chips. It is also important the type of execution: digital, analog or hybrid. At digital execution, without regard to the row of advantages (advanced technologies, high exactness, easy integrations, possibility of storage of weight coefficients in RAM), such disadvantages are as a necessity of converting of analog signals, slowness and relative complication of calculations, and accordingly, complex devices. The advantages of analog execution are high information processing speed and possibility of high-density elements. However, they have disadvantages: it is hard to receive high exactness, parameters variation at production, different characters of interference, that distorts an useful signal, complication of storage of weight coefficients and organization of some operations (multiply, for example, et cetera).

Considerable results, to our mind, for creation of ANN are development of «equivalence» models and development of the proper «equivalence» paradigm [1], which allow to describe the functioning processes, learning algorithms, recognition, explain the processes dynamics in ANN, ground perspective hardware representations. Computer simulation results of «equivalence» neural networks models (ENNM) have showed their efficiency and substantial advantages: increase of capacity to (2.5 – 4.0)N; where N is neurons amount, the possibility of spatially invariant recognition of very correlated 2D- and 1D-patterns [2, 3]. But theoretical foundation of new «equivalence» paradigm requires and new hardware tools with the highly productive simultaneous adaptive processing and adopted biological motivated principles and mechanisms. At creation of technical models of neurons an ultimate goal is development of functional elements with properties of the real neurons. Considerable foundation for development of the proper hardware tools and design of the newest macroelement base was expansion of scalar neurobiologic (NBL) and creation of mathematics of matrix neurobiologic with its base operations of the normalized equivalences (nonequivalence) of two vectors, «equivalence» of spatial functions of 2D-patterns [2, 3] and whole family of new «equivalence» operations on the basis of the use of summarizing operations of continuous fuzzy and neuro-fuzzy logic: fuzzy negation, t-norm and s-norm [4]. It is possible to design neurons macroelement base on the basis of optical and optoelectronic technologies. The last allows to work out the problems of coupling, density et al. But such optoelectronic models for the equivalence paradigm, which are described in work [5] have disadvantages: only some

equivalence and nonequivalence of scalar, but not vector information operations are realized, limited exactness and limited possibility of input number increase. Realization of normalized equivalence or nonequivalence are considered very little, except paper [6]. But synthesis, design of hardware representations of normalized equivalence or nonequivalence of two vectors (or even matrices) are the most actual task. In paper [6] an approach to realize complement dual neuron elements - neuron equivalentor/nonequivalentor was offered. We used conception of pulse-time encoding, as in works [7]. Advantages of such biologically motivated conception are pulse-time (PWM or PPM) principle of signals and variables and operands encoding. Signals at the output of such neurons can be both digital and analog, or hybrid, and also with two complement outputs. Then they realize principle of dualism which gives a number of advantages. Therefore the purpose of this work is subsequent research and perfection of such complement dual neuron elements (NE).

Short theoretical ground and structured design

The weighing coefficients of synapse connections matrix of equivalence models are determined through the normalized equivalence of f, namely [8, 9]:

$$T_{ij}^{0} = \frac{1}{M}\sum_{m=1}^{M}(S_m^i \sim S_m^j) = f(\vec{S}^i, \vec{S}^j), \qquad (1)$$

where S_m^i, S_m^j are proper values of i-th and j-th neuron of m-th standard learning pattern, $\vec{S}^i$ and $\vec{S}^j$ are vectors from all i-th or j-th components of all set from M vectors, whether

$$T_{ij}^{\beta} = \frac{1}{M}\sum_{m=1}^{M}(|\beta_m| \sim S_m^i \sim S_m^j), \qquad (2)$$

where β_m is vectors equivalence coefficient, and also it is the normalized equivalence of f vectors, that

$$\beta_m = f(\vec{X}, \vec{S}^m) = \frac{1}{N}\sum_{i=1}^{N}(S_i^m \sim X_i^{inp}). \qquad (3)$$

Formulas for the neurons initial signals calculation in the equivalence models also taken to determination of the normalized equivalence of f, namely:

$$X_j^{out}(t+1) = \varphi_j\left[f(\vec{T}_j^{0/\beta}, \vec{X}_{(t)}^{inp})\right], \qquad (4)$$

where $\vec{T}_j^{0/\beta}$ is a j-th vector-column from a matrix $\mathbf{T}^{0/\beta}$, and $\vec{X}^{inp}$ is an input vector [9]. In addition, it is possible to show many other formulas, which are used in the equivalence models paradigm and based on calculations of the normalized equivalence or nonequivalence of vectors or matrices [2, 8, 9]. It considerably simplifies realization of such f operations, as all of equivalence types, namely $(\sim)$, $(\overset{+}{\sim})$, $(\overset{\vee}{\sim})$, are taken to one. Mathematical formulas for calculation of f and $\overline{f}$, or $\tilde{e}(\vec{x}, \vec{w})$ and $n\tilde{e}(\vec{x}, \vec{w})$ are showed in paper [6]. We will mark also, that in works [5, 6] it is showed that set of operations, normalized equivalence and nonequivalence is the functional complete system of continuous logic functions. Therefore f realizing from vector information is very actual. We will designate f various types of operations $(\sim)$, $(\overset{+}{\sim})$, $(\overset{\vee}{\sim})$ or their generalizations [4]; ${}^{t,s}E'(a,b) = (a t b)s(\bar{a} t \bar{b})$ by character $(\sim)$ for simplicity. Let vectors $\vec{X}$ and $\vec{W}$ have dimension $N = k \cdot Q$. For every i-th $(i \in 1 \div k)$ subvector $\vec{X}_i$ and i subvector $\vec{W}_i$, the dimension of which equal to Q, it is possible to calculate

$$f_i(\vec{x}_i, \vec{w}_i) = \frac{1}{Q}\sum_{l=1}^{Q}(x_i^l \sim w_i^l) = \tilde{e}_i(\vec{x}_i, \vec{w}_i).$$

Then it is possible to show that:

$$f(\vec{x}, \vec{w}) = \frac{1}{k}\sum_{i=1}^{k} f_i(\vec{x}_i, \vec{w}_i) = \frac{1}{k}\sum_{i=1}^{k}(f_i \sim 1) = \tilde{e}(\vec{f}_k, \vec{1}_k), \qquad (5)$$

where $\vec{f}_k$ and $\vec{1}_k$ are vectors of K dimension, the components of which are equal f_i and "1" accordingly.

Like: $\overline{f}(\vec{x}, \vec{w}) = n\tilde{e}(\vec{f}_k, \vec{0}_k)$. Hence, for increase of vectors dimension, given at inputs of our complemental-dual NE (CDNE), it is possible to use base analogical CDNE of less dimension. Many stage dendrogram is built for this purpose (fig. 1). Thus at inputs of second and the senior stages with vectors of signals $\{\tilde{e}^1, \tilde{e}^2, \ldots \tilde{e}^k\}$ or $\{n\tilde{e}^1, n\tilde{e}^2, \ldots n\tilde{e}^k\}$ it is necessary to give tuning vectors $\{1^1, 1^2, \ldots 1^k\}$ or $\{0^1, 0^2, \ldots 0^k\}$.

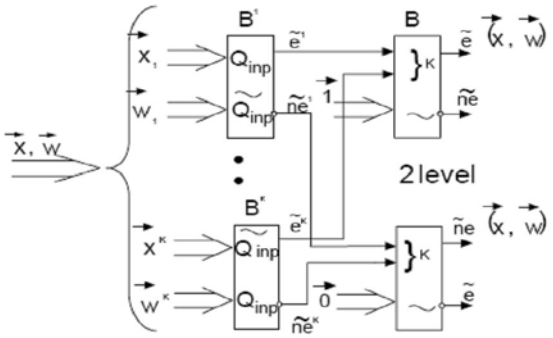

Fig. 1. Many stage CDNE

Thus, for realization of hierarchical tree structure of CDNE of greater dimension we can utilize as base CDNE (BCDNE) of less dimension with operation or normalized equivalence ẽ/(f) or with operation of normalized nonequivalence $n\tilde{e}/(\overline{f})$. If such BCDNE will have two complement outputs, it gives yet greater possibilities, although it is justified not always. Especially at the first stages of hierarchical structure. Better always it to do in the last stage, it can be done both in the base block and with use of additional block (but expenses grow). But reservation and vitality of such systems are increased.

Designing of the base CDNE

The generalized structure of model of neuron, and functional diagram of BCDNE are represented in fig. 2. It consists of N blocks which execute a scalar operation $(\not\sim)$ nonequivalence of i-th component of vectors $\vec{x}^k$ and $\vec{w}^k$, for example:

$$(x_i \not\sim w_i) = |x_i - w_i| = \max(x_i, w_i) - \min(x_i, w_i).$$

In paper [10] we offered blocks for sorting of analog signals (photodiode photocurrents) which execute necessary operations $\max(x_i, w_i)$ and $\min(x_i, w_i)$. They are realized on the basis of photocurrent mirrors on the field effect transistors the amount of which does not exceed 9 – 13 (as evidently from fig. 3, a). In Fig. 3b the time diagrams of such block is represented.

Thus at analog inputs (amplitude code representation of photocurrent or currents) a necessity for the block for transformation of width impulses to amplitude (current) falls off. It is needed to have a block of subtraction of currents and summator-normalizer only, whether summators and block of subtraction.

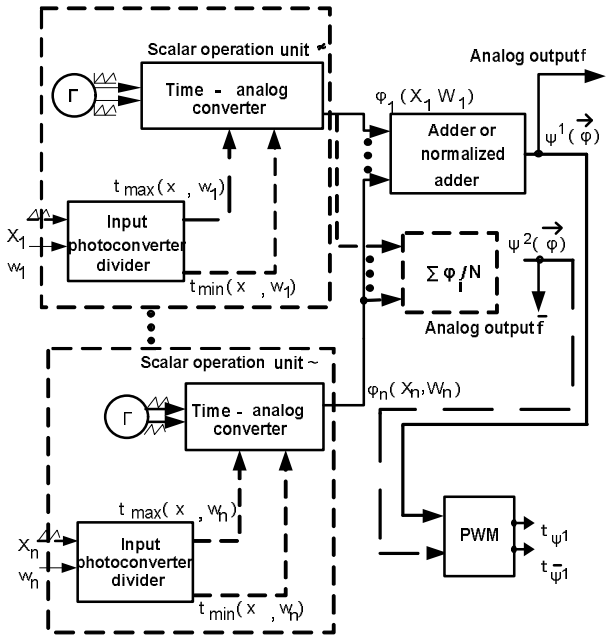

Fig. 2. Functional structure BCDNE for input vector realization

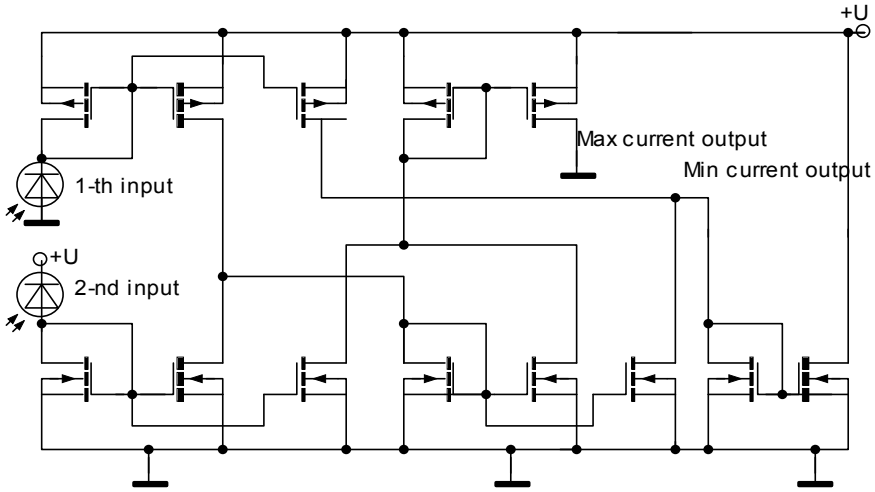

Fig. 3, a. 2x2 sorting circuit

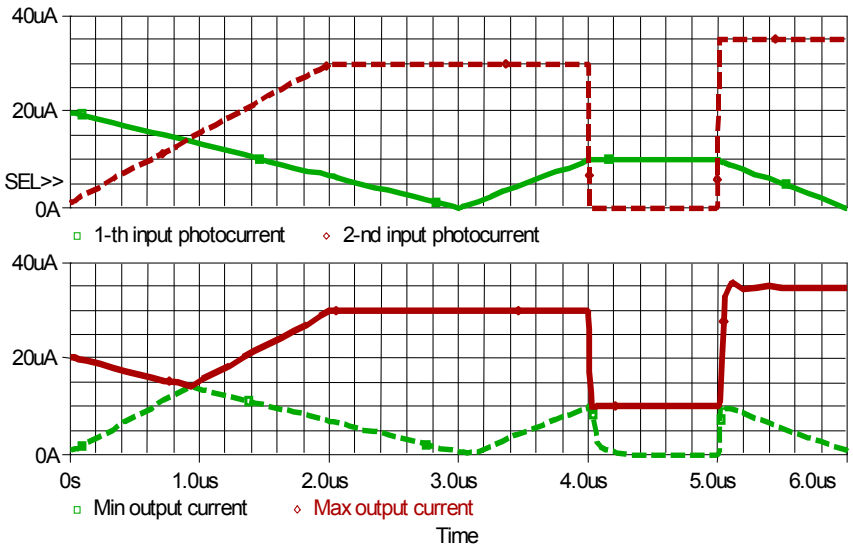

Fig. 3, b. Simulation results of 2x2 sorting circuit

That we realize circuit after formulas:

$$\tilde{ne}(\vec{x},\vec{w}) = \frac{1}{N}\sum_{i=1}^{n}\max_i(x_i, w_i) - \frac{1}{N}\sum_{i=1}^{n}\min_i(x_i, w_i), \quad (6)$$

$$\text{or} \quad \overset{\pm}{n\tilde{e}}(\vec{x},\vec{w}) = \sum_{i=1}^{N}\left(\frac{\max(x_i, w_i) - \min(x_i, w_i)}{N}\right). \quad (7)$$

To realize the operation of f or $\tilde{e}(\vec{x},\vec{w})$ it is possible also to use formulas:

$$\overset{\pm}{\tilde{e}}(\vec{x},\vec{w}) = 1 - \frac{1}{N}\sum_{i=1}^{N}\max(x_i, w_i) + \frac{1}{N}\sum_{i=1}^{N}\min(x_i, w_i). \quad (8)$$

We will mark, that on a current mirror more easily to execute these operations of addition or subtraction of currents. At the use of pulse-width coding in BCDNE it is possible to use a circuit, resulted in papers [6, 7, 10], that contains one photodiode and 7 transistors, and input pulse-width variables x_i, w_i.

On transistors current mirrors threshold photoconversion is performed and it can do the operation «AND» and «OR», that necessary for the selection of max and min duration of impulses. If electric inputs are used, it is necessary only two logical elements, namely element «AND» and element «OR», which easily to realize on field transistors, it is needed not less than 8 transistors.

Design of two-stage circuit of CDNE with pulse-time encoding

For design of two-stage circuit of CDNE non-equivalentor $\tilde{ne}$ with Q = 8 was chosen, it has two PWM at output which form two impulses, durations of which are proportional to normalized nonequivalence $\tilde{ne}$ and to equivalence $\tilde{e}$:

$$t_{\Psi 1} \sim \tilde{ne}; \quad t_{\overline{\Psi} 1} \sim \tilde{e}(\{\vec{x}\}^{Q=8}, \{\vec{w}\}^{Q=8}).$$

Number k of such BCDNE in the first stage we chosen equal to 8, and we designed circuit of CDNE with 64 component vectors. Simulation of separate BCDNE with 8-component input vectors with time-pulse coded values of component (for simplification all components are $x_{i\in 1\div 8} = t_1$, $w_{i\in 1\div 8} = t_2$): at saw amplitude $A_0 = 6.25\mu a$ in knots φ_i, a scope of saw of PWM: $A_{PWM} = 6.25\times 8 = 50\mu a$, supply voltage $U_{vcc} = (3\div 3,7)V$, calculation error of $n\tilde{e}(\vec{x},\vec{w})$ does not exceed 1÷2 % at calculations period $T_{\Sigma} = 110\mu s$ and $T_{Saw} = T_{PWM} = 100\mu S$. For example, at $t_1 = 85\mu s$, $t_2 = 45\mu s$ output signals were $t_{\varphi} = n\tilde{e} = 40.005\mu s$; $t_{\tilde{\varphi}} = \tilde{e} = 60.52\mu s$. At $t_1 = 85\mu s$, $t_2 = 75\mu s$, output signals were $t_{\varphi} = n\tilde{e} = 10.1\mu s$; $t_{\tilde{\varphi}} = \tilde{e} = 93.2\mu s$. At $t_1 = 85\mu s$, $t_2 = 15\mu s$ and accordingly $t_{\varphi} = n\tilde{e} = 69.885\mu s$; a $t_{\tilde{\varphi}} = \tilde{e} = 31.21\mu s$. (fig. 4). Consumption power of base block did not exceed 1mW (≈ 0.7mW) in an experiment.

Simulation results of the two-stage CDNE with pulse-time coded signals prove correct operation of the CDNE with 64 inputs. Form of the sawtooth currents was a bit changed for more reliable functioning. The circuit consists of 9 base BCDNE and general consumption power will not exceed 10mW $(U_{vcc} = (3\div 4)V)$. CDNE can execute different operations: $n\tilde{e}$ and $\tilde{e}$ et al. Calculation error of CDNE at $\tilde{E}(\vec{x}^{64}, \vec{w}^{64})$ by means of realization of operations $n\tilde{e}^k$ in the first and second stages, is about $1\div 3\%$. For example, at signals $n\tilde{e}^i$ as impulses with duration $t_{n\tilde{e}} = 9.5\mu s$. at input of the second stage (result from $t_{Xi} = 15\mu s$. and $t_{Wi} = 85\mu s$) on the output of the 2-th stage there is signal duration $t_{n\tilde{e}} = 69.05\mu s$. Thus the signal of DOUT has duration $t_{\tilde{e}} = 32\mu s$. And the result is the same for different connections of outputs of 1-th stage to inputs of second stage and different tuning (fig. 5). Processing cycle $T_{proc} \approx 0,1ms$, although it can be diminished. A hierarchical tree structure works as a conveyer.

For two stages in spite of delay t_d mean operation time is equal T.

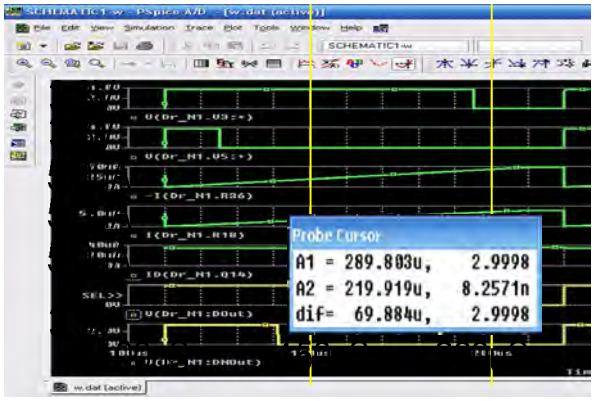

Fig. 4. Time diagrams OECDNE

Thus, it is shown, that with use of our approach, it is possible to create CDNE with a greater dimension, up to N=512 (64*8=512), using either a 3-stage circuit (73 base) or 2-stage (at Q=23) with the general amount of base elements equal to 24. Thus even at the amount of base components equal to 100 total power will be less than 1W.

Conclusions

Optoelectronic complement dual neuron element (OECDNE) with a hierarchical (pyramidal) structure on the basis of neurons with time-pulse coded signals on inputs and outputs was developed by us. Consumption power of the 64-input OECDNE does not exceed 10 mW at supply voltage U= 3÷4 V, and processing time can be at the level of 10 – 100 μs at insignificant error

1÷5 % at calculations of normalized equivalence and nonequivalence.

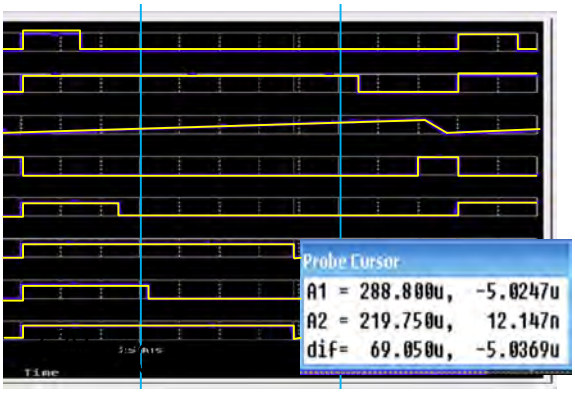

Fig. 5. Time diagrams OECDNE

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Надійшла до редколегії 14.11.2011

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ОПТОЭЛЕКТРОННЫЕ КОМПЛЕМЕНТАРНО-ДУАЛЬНЫЕ НЕЙРОННЫЕ ЭЛЕМЕНТЫ ДЛЯ РЕАЛИЗАЦИИ НОРМАЛИЗОВАННЫХ ВЕКТОРНЫХ ОПЕРАЦИЙ ЭКВИВАЛЕНТНОСТИ И НЕЭКВИВАЛЕНТНОСТИ

В.Г. Красиленко, А.И. Никольский

В статье показаны преимущества эквивалентностных моделей нейронных сетей, базирующихся на матрично-векторных процедурах и вычислении нормализованных операций «эквивалентности» «неэквивалентности» двух векторов. Для реализации этих операций предложены оптоэлектронные комплементарно-дуальные нейронные элементы с иерархической наращиваемой структурой на основе базовых компонентов. Продемонстрированы результаты моделирования базовых компонентов на основе токовых зеркал и нейронных элементов в целом с время-импульсным представлением сигналов. Схемы позволяют обрабатывать векторы размерностью до 512 элементов за десятки микросекунд при потребляемой мощности до 1 Вт.

Ключевые слова: *оптоэлектронные элементы, нейронные сети, времяимпульсно-кодированные сигналы, матрично-векторные вычисления, операции эквивалентности и неэквивалентности, фототоковые зеркала, непрерывная логика.*

ОПТОЕЛЕКТРОННІ КОМПЛЕМЕНТАРНО ДУАЛЬНІ НЕЙРОННІ ЕЛЕМЕНТИ ДЛЯ РЕАЛІЗАЦІЇ НОРМАЛІЗОВАННИХ ВЕКТОРНИХ ОПЕРАЦІЙ ЕКВІВАЛЕНТНОСТІ ТА НЕЕКВІВАЛЕНТНОСТІ

В.Г. Красиленко, О.І. Нікольський

У статті показані переваги еквівалентностних моделей нейронних мереж, що базуються на матрично-векторних процедурах і обчисленні нормалізованих операцій "еквівалентності" "нееквівалентності" двох векторів. Для реалізації цих операцій запропоновані оптоелектронні комплементарно-дуальні нейронні елементи з ієрархічною структурою на основі базових компонентів. Продемонстровані результати моделювання базових компонентів на основі струмових дзеркал і нейронних елементів в цілому з часо-імпульсним представленням сигналів. Схеми дозволяють обробляти вектори розмірністю до 512 елементів за десятки мікросекунд при споживаній потужності до 1 Вт.

Ключові слова: *оптоелектронні елементи, нейронні мережі, часоімпульсно-кодовані сигнали, матрично-векторні обчислення, операції еквівалентності та нееквівалентності, фотострумові віддзеркалювачі, неперервна логіка.*